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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _04 May 2004_.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-15_ is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-3 and 5-15_ is/are rejected.

7)☒ Claim(s) _4_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _04 May 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

The claims are objected to because they include reference characters

which are not enclosed within parentheses.

5   Reference characters corresponding to elements recited in the detailed

description of the drawings and used in conjunction with the recitation of the

same element or group of elements in the claims should be enclosed within

parentheses so as to avoid confusion with other numbers or characters which

may appear in the claims. See MPEP § 608.01(m).

10

Claims 9 and 13 are objected to because of the following informalities:

Claim 9, line 11 discloses "the logic". There is no antecedent basis for this

limitation, as such it is suggested that applicant change "the logic" to --logic--.

Claim 13, lines 6-7 states "the output port". There is no antecedent basis

15   for a single output port. Therefore, it is suggested applicant change "the output

port" to "an output port".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

20   The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and
process of making and using it, in such full, clear, concise, and exact terms as to enable any
person skilled in the art to which it pertains, or with which it is most nearly connected, to make
and use the same and shall set forth the best mode contemplated by the inventor of carrying
25   out his invention.

Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the

5   time the application was filed, had possession of the claimed invention.

Claim 8, line 6 states "the nodes E, F and H are on a level of the hierarchy directly below the level of the node B." In figures 6A and 7 node E is on the same level, level N, as node B. Therefore, there is no support in the specification for the limitation of claim 8, line 6.

10

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

15   Claims 1-3, 5-7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed (U.S. Patent 6,272,141 B1).

Regarding claim 1, Reed discloses "an interconnect structure, comprising: a plurality of interconnected nodes, including distinct nodes A and E

20   (figure 3A, element 324 acts as applicant's node A, element 332 acts as applicant's node E);

a routing logic associated with the nodes (col. 20, lines 24-28 where this is

describing a generic node setup), the routing logic for routing data selectively

among the interconnected nodes (col. 8, lines 52-55);

the nodes A and E being positioned in the interconnect structure so that

5   node A cannot route data to the node E, the node E cannot route data to the

node A (figure 3A, where it is clear from the data path lines that element 324

cannot route data to element 332 and vice versa), and no node exists in the

interconnect structure that can have data routed directly to it from both the node

A and the node E (figure 3A, where it is again clear that no node can have data

10   sent to it directly from elements 324 or 332); and

a logic included as part of said routing logic and associated with the node

A that uses information concerning routing of data through the node E to route

data through the node A (col. 8, lines 52-55 whereby communicating control of

transmission message data with other nodes by a given node allows elements

15   324 and 332 to communicate this control information with each other as well)."

However, Reed explicitly lacks nodes A and E having "the node A having

a plurality of data input ports, a plurality of data output ports, a control signal

output port; and the node E having a plurality of data input ports, a plurality of

data output ports, a control signal output port."

20   Although Reed does not explicitly disclose the plurality of input ports,

plurality of output ports, and control signals in each node in figure 3A, figure 2

elements 210 and 212 show the input ports, elements 220 and 222 show the

output ports, and element 224 shows a control output, thus it is reasonable to

assume that each node of figure 3A will have a plurality of input ports, plurality of

output ports, and a control output even if it is not explicitly drawn.

It would have been obvious to one with ordinary skill in the art at the time

of invention to include the plurality of input and output ports and control signal

5   output port with the nodes for the purpose of sending control information about

message transmissions to other nodes in the interconnect. The motivation for

sending control information to other nodes about message data is so that each

node receives only one message at a time and thus preventing data contention

(Reed, col. 8, lines 63-65).

10

Regarding claim 2, Reed discloses "an interconnect structure in

accordance with claim 1 wherein: the plurality of interconnected nodes includes a

node F distinct from the nodes A and E (figure 3A, element 330 is node F), the

node F...a control signal output port (figure 3A, the dashed line coming out of

15   element 330 represents a control signal coming from a control signal port); and

the nodes A and F are positioned in the interconnect structure so that the node A

cannot route data to the node F, the node F cannot route data through the node

A (figure 3A, where it is clear that elements 324 and 330 cannot route data to

one another), and no node exists in the interconnect structure that can receive

20   data directly routed both from the node A and the node F (figure 3A, where it is

again clear that no node can receive data directly from both elements 324 and

330); and the logic associated with the node A uses information concerning

routing of data through the node F to route data through the node A (col. 8, lines

52-55 whereby communicating control of transmission message data with other

nodes by a given node allows elements 324 and 330 to communicate this control

information with each other as well)."

However, Reed explicitly lacks node F "…having a plurality of data input

5   ports, a plurality of data output ports…" As with claim 1, Reed does disclose in

figure 2 elements 210 and 212 that show the input ports and elements 220 and

222 that show the output ports, thus it is reasonable to assume that each node of

figure 3A will have a plurality of input ports and plurality of output ports even if it

is not explicitly drawn.

10   It would have been obvious to one with ordinary skill in the art at the time

of invention to include the plurality of ports with the interconnect of claim 1 for the

same reasons and motivation as in claim 1.

Regarding claim 3, Reed discloses "an interconnect structure in

15   accordance with claim 2 wherein: the plurality of interconnected nodes includes a

node B distinct from the nodes A, E and F (figure 3A, element 322 acts as

applicant's node B); and a logic associated with node B included as part of the

routing logic (col. 20, lines 24-28 where this is describing a generic node

setup)… the control signal z containing information concerning routing

20   possibilities through the nodes B, F and E, and the logic associated with the node

A for routing of data through the node A depending at least in part on information

concerning routing of data through the nodes B, F and E (col. 8, lines 52-55

whereby communicating control of transmission message data with other nodes

by a given node allows elements 322, 330, 324, and 332 to communicate this

control information with each other as well)."

However, Reed explicitly lacks "the node B having a plurality of data input

ports, a plurality of data output ports, and a control signal output port... being

5   capable of sending a control signal z to the node A..."

As with previous claims, Reed does disclose in figure 2 elements 210 and

212 that show the input ports, elements 220 and 222 that show the output ports,

and element 224 that shows a control output, thus it is reasonable to assume that

each node of figure 3A will have a plurality of input ports, plurality of output ports,

10   and a control output even if it is not explicitly drawn.

It would have been obvious to one with ordinary skill in the art at the time

of invention to include the plurality of ports with the interconnect of claim 1 for the

same reasons and motivation as in claim 1.

15   Regarding claim 5, Reed discloses "an interconnect structure comprising:

a plurality of nodes including distinct nodes A, B and C, the nodes A and B

being both positioned to send data to the node C (figure 3A, element 324 acts as

applicant's node A, element 322 acts as applicant's node B, and element 320

acts as applicant's node C);

20   a plurality of interconnect lines selectively coupling the nodes of the

interconnect structure (figure 3A, all the data paths between the nodes);

a routing logic associated with the node B capable of sending data to the

node C and sending a control signal to the node A that can inform the node A

that the node A is allowed to send a message to the node C (col. 8, lines 52-55

whereby communicating control of transmission message data with other nodes

by a given node allows elements 320 and 332 to communicate this control

information with each other as well)."

5   However, Reed explicitly lacks "a control signal carrying line connected

from the node B to the node A for carrying control signals from the node B to the

node A..."

Although Reed does not explicitly disclose the control signal in each node

in figure 3A, figure 2 element 224 shows a control output for a generic type node,

10   thus it is reasonable to assume that each node of figure 3A will have a control

output even if it is not explicitly drawn.

It would have been obvious to one with ordinary skill in the art at the time

of invention to include the control signal output port with the nodes for the

purpose of sending control information about message transmissions to other

15   nodes in the interconnect. The motivation for sending control information to other

nodes about message data is so that each node receives only one message at a

time and thus preventing data contention (Reed, col. 8, lines 63-65).

Regarding claim 6, Reed discloses the interconnect of claim 5 and "the

20   node C has a plurality of input ports (figure 3A, element 320 has a plurality of

inputs from other nodes)..."

However, Reed explicitly lacks "...data from the nodes A and B arrive at

the node C concurrently so that all of the input ports of the node C receive

messages simultaneously." Although Reed does not explicitly state that the data

arrives simultaneously, it can be reasonably assumed from figure 3A that node C

(element 320) can receive data from element 324 and element 322 as the inputs

from each node are independent of one another and thus data sent from either or

5   both nodes can arrive simultaneously.

It would have been obvious to one with ordinary skill in the art at the time

of invention to have the inputs of node C receive data simultaneously with the

interconnect of claim 5 for the same reasons and motivation as in claim 5.

10   Regarding claim 7, Reed discloses the interconnect of claim 6 and "the

plurality of nodes includes distinct nodes A, B, C, D, E, F and H (figure 3A,

element 324 acts as node A, element 322 acts as node B, element 320 acts as

node C, element 332 acts as node E, element 330 acts as node F, element 326

acts as node D, and element 328 acts as node H)..."

15   However, Reed explicitly lacks "the node C is capable of simultaneously

sending data from the node A to the node D, and capable of sending data form

the node B to the node H."

Although Reed does not explicitly state that the data arrives

simultaneously, it can be reasonably assumed from figure 3A that node C

20   (element 320) can transmit data to element 326 and element 328 as the outputs

from node C are independent of one another and thus data sent to either or both

nodes D and E can arrive simultaneously.

It would have been obvious to one with ordinary skill in the art at the time

of invention to have the outputs of node C send data simultaneously with the

interconnect of claim 5 for the same reasons and motivation as in claim 5.

5   Regarding claim 9, Reed discloses "an interconnect structure comprising:

a plurality of nodes...including the distinct nodes A, B and C, and a

collection of interconnect lines selectively coupling the nodes (figure 3A, element

324 acts as node A, element 322 acts as node B, and element 320 acts as node

C);

10   the node C having a plurality of message input ports, the nodes A and C

positioned in the structure so that A can route a data packet to C (figure 3A

where element 320 has a plurality of inputs and can receive data from element

324);

the nodes B and C positioned in the structure so that B can route a data

15 packet to C (figure 3A where element 320 can receive packets from element

322)...

logic at the node A using the control signal from node B to route

messages (col. 8, lines 52-55 whereby communicating control of transmission

message data with other nodes by a given node allows elements 324 and 332 to

20 communicate this control information with each other as well)..."

However, Reed explicitly lacks each node "adapted to generate a control

signal" and "the nodes A and B positioned in the network so that B can send a

control signal to A; the node B routing a message MB to C; the node A routing a

message MA to C to arrive at concurrently with MB; all input ports of C

concurrently receiving a message."

Although Reed does not explicitly disclose the control signal in each node

in figure 3A, figure 2 element 224 shows a control output for a generic type node,

5   thus it is reasonable to assume that each node of figure 3A will have a control

output even if it is not explicitly drawn.

Further, it is implied by the data paths drawn between the nodes that

messages can be sent from one node to another, and although Reed does not

explicitly state that the data arrives concurrently at node C, it can be reasonably

10   assumed from figure 3A that node C (element 320) can receive data from

element 324 and element 322 as the inputs of node C are independent of one

another and thus data sent to either or both inputs can arrive simultaneously.

It would have been obvious to one with ordinary skill in the art at the time

of invention to include the control signal output port with the nodes for the

15   purpose of sending control information about message transmissions to other

nodes in the interconnect. The motivation for sending control information to other

nodes about message data is so that each node receives only one message at a

time and thus preventing data contention (Reed, col. 8, lines 63-65).

20   Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Reed (U.S. Patent 6,272,141 B1) in view of Yang et al. (U.S. Patent

5,940,389).

Regarding claim 10, Reed discloses "an interconnect structure comprising:

a plurality of interconnected nodes including a node C having a first input

port and a second input port and a first and second output port (figure 3A,

element 320 acts as node C where the first input and first output ports are the

5   ports on the top and the second input and second output ports are the ports on

the bottom);

and a routing logic included within the interconnect structure

However, Reed lacks what Yang discloses, "a plurality of output ports that

are accessible from the second input port but not from the first output port (figure

10   10, where if we take the first node of stage 0, which can represent element 320

of Reed, we see two input ports and two output ports, the second input port, if

followed, leads to a plurality of output ports that are not accessible from the first

input port)..." and the routing logic is "to assure that when a message MA arrives

at the first input port and simultaneously a message MB arrives at the second

15   input port there is a path through the second output port to a target destination

for message MA and a path through the first output port to a target destination for

message MB (figure 10, where the first node of stage 0 can receive input from

two ports, like element 320 of Reed, and as indicated by the data paths drawn

can send concurrent messages to two different nodes, such as elements 326 and

20   328 of Reed)."

It would have been obvious to one with ordinary skill in the art at the time

of invention to include the assurance of messages being routed from an input to

an output for the purpose of creating a non-blocking set of nodes (Yang, col. 7,

lines 3-31). The motivation for having a non-blocking set of nodes is the

advantage of having a plurality of data being transported through the nodes

without any being lost or blocked because of contention issues.

5   Regarding claim 11, Reed and Yang disclose the interconnect of claim 10.

However, Reed lacks what Yang further discloses, "said routing logic assumes

that message MB is not blocked from using the first output port and message MA

is not blocked from using the second output port (col. 7, lines 3-31 where by the

very nature of the node setup, the outputs are not blocked)." It would have been

10   obvious to one with ordinary skill in the art at the time of invention to include the

non-blocking with the interconnect of claim 10 for the same reasons and

motivation as in claim 10.

           Regarding claim 13, Reed discloses "an interconnect structure comprising:

15   a plurality of interconnected nodes including nodes A, B, C, D, and H

(figure 3A, element 324 acts as node A, element 322 acts as node B, element

320 acts as node C, element 326 acts as node D, and element 328 acts as node

H), each of the nodes A, B, C, D and H having a plurality of input ports and a

plurality of output ports (figure 2 elements 210 and 212 show the input ports and

20   elements 220 and 222 show the output ports of a generic node in the

interconnect), and node C being positioned to receive messages from A and B

and to route messages to D and H (figure 3A shows element 320 being

positioned to receive data from elements 324 and 322 and send data to elements

326 and 328);

a plurality of interconnect structure output ports including [an] output port

that is accessible from node C but not node H (figure 3A where as seen there are

5   a plurality of output ports on each node and there is an output port from element

320 to element 326 that is clearly not accessible from element 328);

a routing logic included within the interconnect structure (col. 20, lines 24-

28 where this is describing a generic node setup)..."

However, Reed lacks what Yang discloses, the routing logic is "to assure

10   that when node A sends a message MA to node C and concurrently node B

sends a message MB to node C, then node C can route MA through node D to a

target interconnect structure output port for MA and node C can route MB

through node H to a target interconnect structure output port for MB (figure 10,

where the first node of stage 0 can receive input from two ports, like element 320

15   of Reed, and as indicated by the data paths drawn can send concurrent

messages to two different nodes, such as elements 326 and 328 of Reed)."

It would have been obvious to one with ordinary skill in the art at the time

of invention to include the assurance of messages being routed from an input to

an output for the purpose of creating a non-blocking set of nodes (Yang, col. 7,

20   lines 3-31). The motivation for having a non-blocking set of nodes is the

advantage of having a plurality of data being transported through the nodes

without any being lost or blocked because of contention issues.

Regarding claim 14, Reed and Yang disclose the interconnect of claim 13. However, Reed lacks what Yang further discloses, "said routing logic assures that message MB is not blocked from node H, and message MA is not blocked from node D (col. 7, lines 3-31 where by the very nature of the node setup, the

5   outputs are not blocked)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the non-blocking with the interconnect of claim 13 for the same reasons and motivation as in claim 13.

Regarding claims 12 and 15, Reed and Yang disclose the interconnects of

10   claims 11 and 14. However, Reed lacks what Yang further discloses, "said routing logic for the routing of messages MA and MB depends in part on QOS criteria (col. 21, lines 26-31 as is known in the art, priority of data is a QoS criteria)." It would have been obvious to one of ordinary skill in the art at the time of invention to include the QoS criteria with the interconnects of claims 11 and 14

15   for the same reasons and motivation as in claims 11 and 14.

Allowable Subject Matter

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations

20   of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments, see Remarks, page 20, paragraph 2, filed 4 May 2004, with respect to objections of claims 11 and 14 have been fully considered and are persuasive. The objection of claims 11 and 14 has been withdrawn.

5   Applicant's arguments, see Remarks, page 20, paragraph 3, filed 4 May 2004, with respect to objections of claims 7, 9-12, and 14 have been fully considered and are persuasive. The objection of claims 7, 9-12, and 14 has been withdrawn.

10   Applicant's arguments, see Remarks, pages 20-25, filed 4 May 2004, with respect to the rejection(s)of claim(s) 1-4, 6-12, and 13-15 under 35 U.S.C. 112 first paragraph, claim 5 under 35 U.S.C. 102(b), and claim 9 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of

15   rejection is made in view of a better understanding of applicant's invention and review of prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Kading whose telephone number is

20   (703) 305-0342. The examiner can normally be reached on M-F: 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Olms can be reached on (703) 305-4703. The

fax phone number for the organization where this application or proceeding is

assigned is 703-872-9306.

Information regarding the status of an application may be obtained from

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5   for published applications may be obtained from either Private PAIR or Public

PAIR. Status information for unpublished applications is available through

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direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

10   free).

Joshua Kading
Examiner
Art Unit 2661

KENNETH VANDERPUYE
PRIMARY EXAMINER

July 15, 2004